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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/750,090	12/29/2000	Jeffery F. Harness	2207/10377	6380
23838 7590 01/19/2007 KENYON & KENYON LLP 1500 K STREET N.W.			EXAMINER	
			DO, CHAT C	
SUITE 700 WASHINGTON, DC 20005			ART UNIT	PAPER NUMBER
			2193	
	,			
			MAIL DATE	DELIVERY MODE
		•	01/19/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action After the Filing of an Appeal Brief

Application No.	Applicant(s)	
09/750,090	HARNESS ET AL.	
Examiner	Art Unit	
Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

The reply filed <u>26 December 2006</u> is acknowledged.

- 1. The reply filed on or after the date of filing of an appeal brief, but prior to a final decision by the Board of Patent Appeals and Interferences, will <u>not</u> be entered because:
 - a. The amendment is not limited to canceling claims (where the cancellation does not affect the scope of any other pending claims) or rewriting dependent claims into independent form (no limitation of a dependent claim can be excluded in rewriting that claim). See 37 CFR 41.33(b) and (c).
 - b. The affidavit or other evidence is not timely filed before the filing of an appeal brief. See 37 CFR 41.33(d)(2).
- 2. The reply is not entered because it was not filed within the two month time period set forth in 37 CFR 41.39(b), 41.50(a)(2), or 41.50(b) (whichever is appropriate). Extensions of time under 37 CFR 1.136(a) are not available.

Note: This paragraph is for a reply filed in response to one of the following: (a) an examiner's answer that includes a new ground of rejection (37 CFR 41.39(a)(2)); (b) a supplemental examiner's answer written in response to a remand by the Board of Patent Appeals and Interferences for further consideration of rejection (37 CFR 41.50(a)(2)); or (c) a Board of Patent Appeals and Interferences decision that includes a new ground of rejection (37 CFR 41.50(b)).

- 3. The reply is entered. An explanation of the status of the claims after entry is below or attached.
- 4. A Other: The applicant argues that the cited reference fails to disclose the structure/limitations detecting opposite logic values of both adjacent bits. The examiner respectfully submits that the argument is clearly presented and addressed in the previous Office action wherein the cited reference clearly disclose an invention of detecting a glitch within data. A glitch is define as a spike or high logic value wherein both adjacent bits are low. Thus, the cited reference must disclose either inherently or expressively a method of detecting opposite logic values of both adjacent bits.

TAN V. MAI PRIMARY EXAMINER

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